

WHAT IS CLAIMED IS:

1. A memory device, comprising:

first and second split wordlines formed on a substrate extending along a first direction separated by prescribed intervals;

a first conductive layer that couples a second electrode of the first ferroelectric capacitor with a first active region at a first side of the second split wordline;

a second conductive layer that couples a second electrode of the second ferroelectric capacitor with a second active region at a first side of the first split wordline; and

first and second bitlines respectively coupled to the active regions at second sides of the respective split wordlines, wherein the second sides of the respective split wordlines are opposite the first sides.

2. The memory device of claim 1, wherein the first and second ferroelectric capacitors comprise:

a first electrode of the first ferroelectric capacitor formed on the second split wordline and a first electrode of the second ferroelectric capacitor formed on the first split wordline;

first and second ferroelectric layers respectively formed on surfaces of the first electrodes of the first and second ferroelectric capacitors; and

second electrodes of the first and second ferroelectric capacitors respectively formed on surfaces of the first and second ferroelectric layers.

3. The memory device of claim 2, wherein the second electrode of the first ferroelectric capacitor and the second electrode of the second ferroelectric capacitor have folded shapes to the split wordlines or the bitlines.

4. The nonvolatile ferroelectric ~~memory~~ device of claim 2, wherein the second electrode of the first ferroelectric capacitor and the second electrode of the second ferroelectric capacitor are symmetrically formed in parallel along the split wordlines.

5. A memory device, comprising:
a semiconductor substrate having a first active region and a second active region spaced apart from each other and extending along a second direction;

first and second split wordlines extending along a first direction across the first and second active regions, respectively;

first and second impurity regions respectively formed in the first and second active regions at both sides of the first and second split wordlines;

first plugs respectively coupled to the second impurity regions through contact holes;

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second plugs respectively coupled to the first impurity regions through the contract holes;

first electrodes of first and second ferroelectric capacitors on the second and first split wordlines, respectively;

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first and second first ferroelectric layers on the first electrodes of the first and second ferroelectric capacitors, respectively;

island shaped second electrodes of the first and second ferroelectric capacitors on surfaces of the first and second ferroelectric layers, respectively;

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first and second conductive layers respectively coupling the second plugs that are coupled to the first impurity regions with the second electrodes of the first and second ferroelectric capacitors; and

first and second bitlines extending along the second direction to cross the first and second split wordlines that are respectively coupled to the first plugs that are respectively coupled to the second impurity regions.

6. The memory device of claim 5, further comprising third plugs between the first and second bitlines and the first plugs.

7. The memory device of claim 6, wherein the first bitline is coupled to the third plug that is coupled to the second impurity region of the first active region through the first plug,

and wherein the second bitline is coupled to the third plug coupled to the second impurity region of the second active region.

8. The memory device of claim 5, wherein the first conductive layer directly connects the second electrode of the first ferroelectric capacitor with the second plug coupled to the first impurity region of the first active region, and wherein the second conductive layer directly couples the second electrode of the second ferroelectric capacitor with the second plug coupled to the first impurity region of the second active region.

9. The memory device of claim 5, wherein the first split wordline is electrically coupled to the first electrode of the second ferroelectric capacitor while the second split wordline is electrically coupled to the first electrode of the first ferroelectric capacitor.

10. The memory device of claim 5, wherein the second electrodes of the first and second ferroelectric capacitors are respectively formed on field regions at two sides of the active regions.

11. The memory device of claim 5, wherein the second electrodes of the first and second ferroelectric capacitors are symmetrically formed in parallel along the first and second split wordlines.

12. The memory device of claim 11, wherein the second electrode of the first ferroelectric capacitor extends from a region between source and drain regions of the second active region to the field region below the first active region, while the second electrode of the second ferroelectric capacitor extends from a region between source and drain regions of the first active region to the field region above the second active region.

13. The memory device of claim 5, further comprising a barrier metal layer formed under the first electrodes of the ferroelectric capacitors.

14. The memory device of claim 5, further comprising:
a cell array having a matrix form of split wordline pairs crossing bitlines;
a wordline driver coupled to the wordlines;
a decoder coupled to the bitlines; and
an output unit coupled to the bitlines, wherein the wordline pairs are each the first and second split wordlines, wherein first and second active regions are asymmetrically positioned.

15. A method for fabricating a device, the method comprising:
defining a first active region and a second active region on a semiconductor substrate;

forming first split wordline across the first active region and a second split
5 wordline across the second active region;

A1 forming first and second source and drain regions in the first and second active
regions, respectively, wherein the source and drain regions are at opposite sides of the first and
second split wordlines;

forming first plugs coupled to the first and second drain regions through a contact
10 hole;

forming second plugs coupled to the first and second source regions through the
contract hole;

respectively forming first electrodes of first and second ferroelectric capacitors
over the second and first split wordlines;

forming ferroelectric layers on the first electrodes;

respectively forming island shaped second electrodes of the first and second
ferroelectric capacitors on surfaces of the first and second ferroelectric layers;

respectively forming first and second conductive layers that couple the second
plugs with the second electrodes of the first and second ferroelectric capacitors; and

forming first and second bitlines across the first and second split wordlines,
20 wherein the first and second bitlines are coupled to the first and second drain regions through
the first plugs.

16. The method of claim 15, wherein the first active region and the second active region are spaced apart from each other and asymmetrically formed each extending in a first direction, and wherein the first electrodes have a folded shape to the first and second wordlines.

17. The method of claim 15, wherein the first electrode of the first ferroelectric capacitor is formed over the second split wordline and an insulating layer is formed therebetween, and wherein the first electrode of the second ferroelectric capacitor is formed over the first split wordline and an insulating layer is formed therebetween.

18. The method of claim 15, wherein forming the second electrodes of the first and second ferroelectric capacitors comprises:

forming a second electrode material layer of the ferroelectric capacitor on an entire surface including the first and second ferroelectric layers; and

selectively removing the second electrode material layer, wherein the second electrode of the first ferroelectric capacitor and the second electrode of the second ferroelectric capacitor are respectively formed on the field regions at both sides of the active region.

19. The method of claim 15, wherein forming the first and second conductive layers comprises:

forming a conductive material layer on the entire surface including the second electrodes of the first and second ferroelectric capacitors; and

selectively removing the conductive material layer to form the first and second conductive layers, wherein the first conductive layer is directly coupled with the second electrode of the first ferroelectric capacitor and the second plug that is coupled to the first source region, and wherein the second conductive layer being directly coupled with the second electrode of the second ferroelectric capacitor and the second plug that is coupled to the second source region.

20. The method of claim 18, further comprising forming third plugs coupled to the first plugs respectively, before forming the first and second bitlines, wherein the first bitline is coupled with the third plug coupled to the first drain region through the first plug, and wherein the second bitline is coupled with the third plug coupled to the second drain region through the first plug.

21. The method of claim 15, further comprising electrically coupling the first split wordline with the first electrode of the second ferroelectric capacitor, and electrically coupling the second split wordline with the first electrode of the first ferroelectric capacitor.

22. The method of claim 15, wherein forming the second electrodes of the first and second ferroelectric capacitors comprises:

forming a second electrode material layer of the ferroelectric capacitors on the entire surface including the first and second ferroelectric layers; and

